Rajinthan Rameshkumar

Electronic & Telecommunication Engineering · University of Moratuwa · NUS Research Intern

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About

Undergraduate researcher in analog and mixed-signal IC design, with tapeout experience across the SKY130 and IHP SG13G2 PDKs. Current projects include a Noise-Shaping SAR ADC (Cadence/SKY130, final-year project) and a 2.4 GHz ΔΣ Fractional-N PLL developed under the IEEE CASS UNIC-CASS program. Research interests span power-efficient analog/RF ICs, photonic integrated circuits, and FPGA-based prototyping; seeking a PhD position to pursue these at the device and system level.

Research Interests:

- Analog and mixed-signal ICs
- RF and high-frequency ICs
- FPGA-based prototyping
- Photonic Integrated Circuits (PICs)
- Power-efficient SoCs
- Motor control systems
- Optoelectronics & Control
- IC layout optimization

Education

University of Moratuwa, Sri Lanka — **Cumulative GPA: 3.77 / 4.0** — 2023 – 2027
B.Sc. Engineering (Hons.) — *Dean's List: Semesters 1, 2, 4*
Electronic and Telecommunication Engineering
Coursework: Analog and Digital Electronics, Signal Processing, Control Systems, Computer Architecture, Communication Systems, Embedded Systems Programming, Data Structures and Algorithms

J/Hartley College, Jaffna, Sri Lanka — 2013 – 2022

- G.C.E. Advanced Level 2021 – Physical Science (Combined Mathematics, Physics, Chemistry)
  Z-score: 2.4978, Island Rank: 158th
- G.C.E. Ordinary Level 2018 – 9As (including Commerce, ICT & Art)
- Served as **Senior Prefect**

Courses & Certifications

- Beginning C++ Programming – From Beginner to Beyond, Udemy
- Mastering Microcontroller and Embedded Driver Development, Udemy
- Introduction to FPGA Design for Embedded Systems, Coursera
- 100 Days of Code: The Complete Python Pro Bootcamp, Udemy

Experience

StarLabs, National University of Singapore (NUS) – Research Intern — Dec 2025 – Present

- Developing a high-torque smart reaction wheel controller for satellite Attitude Determination and Control Systems (ADCS).
- Implementing Field-Oriented Control (FOC) algorithms and sensor interfacing to drive and optimize BLDC motors.

RoboticGen (startup), Colombo, Sri Lanka – Robotics Team Member — Apr 2025 – Jan 2026

- Designed a 4WD system reaching 3 m/s – twice the speed of the previous version – for an open-source micromouse.
- Created STM32F405-powered PCB for motor control, reducing board size by over 40%.
- Implementing PID control algorithms with encoder feedback and sensor integration for maze navigation.

Publications

A 2.4 GHz LC-VCO Fractional-N Phase Locked Loop Open-Source Design in 130 nm BiCMOS — 2026
Accepted at SMACD 2026 (International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design). Presents an open-source ΔΣ Fractional-N PLL with LC-VCO targeting 2.4 GHz WiFi/Bluetooth applications, implemented in the IHP SG13G2 130 nm BiCMOS PDK under the IEEE CASS UNIC-CASS program.

Projects

Very Low Power NS-SAR ADC Jan 2026 – Present
Designing a Noise-Shaping Successive Approximation Register (NS-SAR) Analog-to-Digital Converter optimized for ultra-low-power operation as a final-year academic project, utilizing the SKY130 PDK in Cadence.

2.4 GHz Type-II Fractional-N PLL with LC-VCO Aug 2025 – Present
Designing a 2.4 GHz Type-II $\Delta\Sigma$ Fractional-N Phase-Locked Loop coupled with a Type-IV Cross-Coupled Differential LC-VCO for WiFi/Bluetooth applications, using the IHP SG13G2 PDK under the IEEE CASS UNIC-CASS program. Includes PFD and charge pump design.
GitHub: SkillSurf/frac-n-pll-vco-smacd_2026

Low-Power Two-Stage Operational Amplifier (TinyTapeout) Nov 2025
Designed and taped out a single-ended (SE) two-stage CMOS op-amp achieving 80 dB open-loop gain, 4 MHz unity-gain bandwidth, and 2 nA disable current, using xschem, ngspice, and KLayout within the SKY130 PDK.
GitHub: rajinthanr/ttsky_opamp

4-Way Set-Associative Cache 2025
Implemented a 64 KB 4-way set-associative cache in Verilog with non-blocking MSHR support and LFSR-based replacement policy, synthesized and verified on the DE0-Nano FPGA.
GitHub: rajinthanr/Set-Associative-Cache

Open-Source Micromouse: High-Speed Maze-Solving Robot Nov 2025 – Present
Leading design of an open-source micromouse with STM32F405, PID-based motion control, and encoder feedback for high-speed, low-latency navigation.
GitHub: RoboticGen/obo-mouse-v4

UART Module on DE0-Nano FPGA Apr 2025
Implemented a custom UART block in Verilog at 9600 baud on the DE0-Nano, with transmitter/receiver design, ModelSim simulation, and cross-board hardware verification.
GitHub: rajinthanr/Digital-System-Design

Reconfigurable Gripper for Robotic Autonomous Depalletizing Jan 2025
Developed a robotic end-effector with pneumatic actuation, vacuum pumps, and register-level ARM firmware for real-time control. Integrated ToF sensors and rack-and-pinion drive for adaptive box handling.
GitHub: rajinthanr/End_Effector

High-Speed Line Follower Robot – Dextron 2024 Champion Dec 2024
Designed a two-wheeled robot with STM32F411 achieving speeds exceeding 0.7 m/s using encoder-based PID control and real-time sensor filtering.

Achievements

2nd Runner-Up (3rd Globally) | 20th International Microelectronics Olympiad, Yerevan, Armenia 2025
Competed among 20+ countries including USA, UAE, Germany, and France in microelectronics and EDA.

Champion | IEEE Chips Challenge 2025 – national qualifier, Int'l Microelectronics Olympiad 2025

Champions | SLIIT RoboFest 2025 – Micromouse, University Category 2025

Champions | Dextron 2024 – Fast Line Follower, ITUM 2024

1st Runner-Up | Sri Lankan Robotics Challenge 2022/23 – Electronic Club, University of Moratuwa 2023

2nd Runner-Up | IESL RoboGames 2023 – UoM, IESL, SLT-Mobitel 2023

Champions | UWU Robot Battle 2.0 – Death Race, Uva Wellassa University 2023

1st Runner-Up | All-Island School Robot Competition – Engineering Technology, Ministry of Education 2019

Silver Medal | National Mathematics Olympiad, Category III 2018

Gold Medal ×2 | All-Island Math Quiz Competition – Northern Province representative 2016, 2017

Skills

Programming Languages: C++, C, Python, MATLAB, Verilog, LaTeX, Shell scripting
Microcontrollers: STM32 (F4, H7, F405, F411), ARM Cortex series, ESP32, ATmega2560
EDA / IC Tools: Cadence, xschem, ngspice, KLayout, LTSpice, OSIIC
PDKs: SkyWater SKY130A, IHP SG13G2
FPGA Tools: Intel Quartus Prime, ModelSim
PCB / Mechanical: Altium Designer, SolidWorks
IDEs & Platforms: STM32CubeIDE, Linux
Professional: Leadership, Project Management, Mentoring

Clubs and Organizations

IEEE Circuits and Systems (CAS) Society Student Chapter – *Webmaster* (Dec 2025 – Present). Managing digital presence and technical communications for the University of Moratuwa chapter.

E-Club (Electronic Club) (Jan 2025 – Present) – Active member; photographer/videographer for department events including the Career Fair and AGM.

Yarl IT Hub (Jan 2022 – Present) – Volunteer coordinator; grew a school-level robotics competition from 25 to 50+ teams across two years.

References

Prof. Rohan Munasinghe
Professor, University of Moratuwa
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B.Sc. Eng. (Moratuwa), M.Sc. (Saga), Ph.D. (Saga), CEng., MIE(SL), SMIEEE

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